

MPC8572

High-Performance Integrated MPU

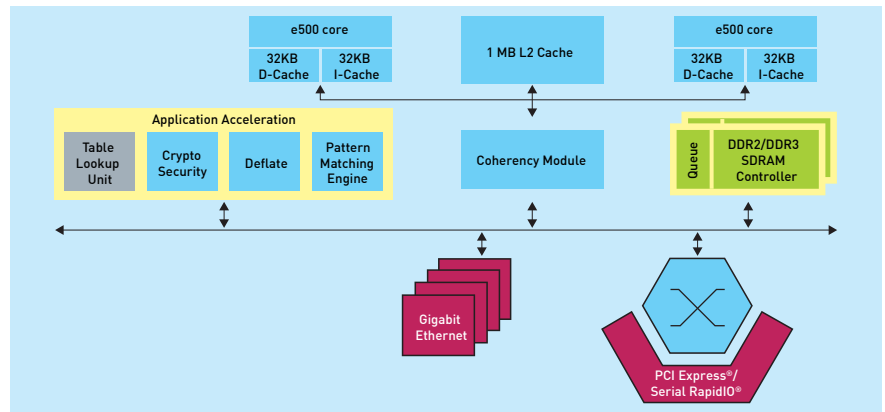


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The 8572 is the first dual core PQIII processor based on the e500 System on Chip platform. It contains two e500v2 cores, (36-bit addressing, 64-bit Floating Point and better MMU compared to e500v1). The 8572 is a milestone product as it is an important step to future Freescale processors. Both traditional OS's and Symmetric Multiprocessing OS's are supported. The processor includes most of the peripherals from the 8548/8641D, some of them enhanced, and adds some extra apps accelerators of its own. Its unique pattern matching engine is able to look for single or nested patterns in a continuous bitstream with no word boundaries issues, programmable in high level and in system updatable. Some of its usage is intrusion detect, virus scan, pattern matching. Deflate engine for "unzipping" compressed data to save CPU cycles. Latest version Security coprocessor, DMA based, for total offloading of the CPU. Four intelligent 10/100/1000 Ethernet controllers eTSEC with SGMII interface to PHYs, one 10/100 Ethernet controller for debug/maintenance thrown in for good measure.

Key Features

- Cores
 - SPE instruction set
 - Three processing units
 - Vector and scalar single precision FPU
 - Double precision FPU
 - MMU design for embedded apps
 - 1MB level 2 cache
 - L2 cache ECC protected
 - 36-bit physical address range
 - Doze, nap and sleep low-power modes
- D-RAM controllers
 - DRII and DDRIII support
 - 64-bit with optional ECC
 - 64Mb...4Gb, D-RAM supported
 - On die termination
 - Cache line, page, bank and superbank interleaving



- PCI Express units
 - Support x8, x4, x2, x1 1.0a links
 - Auto detection of connected lanes
 - Supports single, dual and serial RapidIO
 - OCeaN crossbar switch and two separate 4-channel DMA engines between all external serial busses.
- RapidIO
 - Single Serial RapidIO port 4x/1x multiplexed with PCI Express
- Pattern Matching Engine
 - Regular expression pattern matching
 - Cross packet detection
 - Support for 16k simultaneous patterns
- Table lookup units
 - Each TLU unit has 16 tables of 16 mega entries each up to 64 bytes, 32/64/96/128-bit keys
- Security coprocessor
 - Eight specialized execution engines
 - Four virtual channels
 - DMA driven
- eTSEC
 - 1Gb full duplex 100/10Mb full and half duplex support
 - QoS with eight separate TX and eight separate RX queues
 - VLAN support, with insertion and deletion, individual for each eTSEC
 - IEEE1588 HW support
 - Jumbo frame support
- TCP/IP acceleration, header recognition, IP4 checksum calculation and verification, UDP and TCP checksum and verification
- Multiple MAC address recognition modes, hash or exact
- Local Bus Controller
 - Multiplexed 32-bit data and address bus up
 - Eight chip selects, with programmable burst length, port size and waitstates
 - Three user programmable machines
 - NAND controller

Key Applications

- High end industrial control
- Imaging
- Robotics
- Firewall/VPN
- 3G/4G base stations
- Intrusion/virus detection/prevention

Key Design Tips

- SMP Linux BSP from Freescale
- PPCEVAL-DS-8572 evalboard from Freescale
- Multiple third party support

Service available or already delivered T&R from Manufacturer.
 Tapes are available, but not stocked at Avnet Logistics due to low demand.
 Device supported by or programming equipment, but the socket for this package must be provided by customer.

P/N	Package	Programming	Taping & Reeling	Marking
PPC8572EVTAUJ	1023-ball FCBGA			
PPCEVAL-DS-8572		Tool		