

ISE Foundation 8.1i

Complete Design Solution



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ISE Foundation 8.1 provides everything designers need in a complete logic design environment for all Xilinx FPGA and CPLD products. It is an advanced integrated software technology that offers front-to-back design, but can also be integrated with the industry's leading third-party EDA tool offerings, enabling the customisation of design flows to meet specific project demands.

Key Features

- Easy to use
- Built in tools and wizards
- Intuitive IO assignment, power analysis, timing driven design and HDL simulation
- ISE report and error messages navigate directly to award winning Xilinx support
- Xilinx FMAX technology
 - Solves designers' #1 challenge: timing closure
 - Delivers the fastest implementation for a given design
 - Includes retiming during implementation for a given design
 - Timing driven mapping
 - Global optimisation
 - Logic optimisation and register duplication

- The fastest out-of-the box performance for unconstrained designs
- Performance evaluation mode and Xplorer script
 - Provides 10-37% better performance compared to previous releases of ISE
- No cost, downloadable ISE WebPACK version for CPLDs and low density FPGAs
- ISE Webpack operates on Windows 2000 or XP and on Red Hat Enterprise Linux 3 (32-bit)
- ISE Foundation also on Red Hat Enterprise Linux 3 (64-bit) and Sun Solaris 2.8 or 2.9

Specifications

Design Entry:

- Schematic Editor
- HDL Editor
- State Diagram Editor (for Windows only)
- Xilinx CORE Generator System
- RTL & Technology Viewers
- PACE (Pinout & Area Constraint Editor)
- Architecture Wizards
- Third Party RTL Checker support
- Optional: Xilinx System Generator for DSP
- Optional: Embedded Design Kit (EDK) see page 48

Synthesis:

- XST: Xilinx Synthesis Technology
- Interfaces to:
 - Mentor Graphics Leonardo Spectrum (Integrated/EDIF on Linux)
 - Mentor Graphics Precision RTL (Integrated)
 - Mentor Graphics Precision Physical (EDIF)
 - Synopsys DC-FPGA Compiler (EDIF)
 - Symplify/Pro/Premier (Integrated)
 - Symplicity Amplify Physical Synthesis (EDIF)
 - ABEL (for CPLDs on Microsoft Windows only)

Implementation

- Floor Planner
- Optional: Plan Ahead
- Timing Driven Place & Route
- Incremental Design
- Timing Improvement Wizard
- Xplorer

Programming

- IMPACT/SystemACE/CableServer

Board Level Integration

- IBIS, STAMP and HSPICE*
- ELDO Models (MGT only)

Verification:

- Optional: ChipScope Pro
- Graphical Testbench Editor (Microsoft Windows only)
- ISE Simulator Lite
- Optional for ISE Foundation: ISE Simulator
- ModelSim XE III Starter
- Optional: ModelSim XE III
- Static Timing Analyzer
- FPGA editor with probe
- ChipViewer
- XPower (power analysis)
- Third party equivalency checking support
- SMARTModels for PowerPC and RocketIO
- Third party simulator support

* Whenever RoHS compliance stated, please refer to manufactures documentation for details. Subject to corrections and changes. All prices exclude VAT.