

		Spartan-6 LX FPGAs Optimized for Lowest Cost Logic, DSP, and Memory (1.2 Volt, 1.0 Volt)							Spartan-6 LXT FPGAs Optimized for Low Cost Logic, DSP, and Memory with High Speed Serial Connectivity (1.2 Volt)				
		Part Number	XC6SLX4	XC6SLX9	XC6SLX16	XC6SLX25	XC6SLX45	XC6SLX100	XC6SLX150	XC6SLX25T	XC6SLX45T	XC6SLX100T	XC6SLX150T
Logic Resources	Slices <sup>(1)</sup>	526	1,422	2,278	3,714	6,790	15,782	23,040	3,714	6,790	15,782	23,040	
	Logic Cells <sup>(2)</sup>	3,366	9,101	14,579	23,770	43,456	101,005	147,456	23,770	43,456	101,005	147,456	
	CLB Flip-Flops	4,208	11,376	18,224	29,712	54,320	126,256	184,320	29,712	54,320	126,256	184,320	
Memory Resources	Maximum Distributed RAM (Kbits)	32	90	136	228	401	975	1,358	228	401	975	1,358	
	Block RAM (18K bits each)	8	32	32	52	116	268	268	52	116	268	268	
	Total Block RAM (Kbits) <sup>(3)</sup>	144	576	576	936	2,088	4,824	4,824	936	2,088	4,824	4,824	
Clock Resources	Clock Manager Tiles (CMT) <sup>(4)</sup>	1	2	2	2	4	6	6	2	4	6	6	
I/O Resources	Maximum Single-Ended Pins	120	200	232	264	370	498	498	264	296	396	396	
	Maximum Differential Pairs	60	100	116	132	185	249	249	132	148	198	198	
Embedded Hard IP Resources	DSP48A1 Slices <sup>(5)</sup>	4	16	32	38	58	182	182	38	58	182	182	
	PCI Express® Endpoint Block	—	—	—	—	—	—	—	1	1	1	1	
	Memory Controller Blocks	0	2	2	2	2	4	4	2	2	4	4	
	GTP Low-Power Transceivers	—	—	—	—	—	—	—	2	4	8	8	
Speed Grades	Commercial	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	
	Industrial	-L1, -2	-L1, -2	-L1, -2	-L1, -2	-L1, -2	-L1, -2	-L1, -2	-2	-2	-2	-2	
Configuration	Configuration Memory (Mbits)	1.0	2.0	2.7	4.4	7.7	17.1	28.0	4.4	7.7	17.1	28.0	
	Package	Area (Pitch)	Maximum User I/O: Select IO™ Interface Pins (GTP transceivers)										
	TQG144	20 x 20 mm (0.5 mm)	100	100									
	CSG225	13 x 13 mm (0.8 mm)	120	160	160	160							
	FTG256	17 x 17 mm (1.0 mm)			186	186							
	CSG324	15 x 15 mm (0.8 mm)		200	232	232			174 (2)	174 (4)			
	FGG484	23 x 23 mm (1.0 mm)				264	354	354	354	264 (2)	296 (4)	296 (4)	296 (4)
	FGG676	27 x 27 mm (1.0 mm)					370	498	498		370 (4)	396 (8)	396 (8)

- Notes:
- Each Spartan-6 FPGA CLB contains four LUTs and eight flip-flops.
  - Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
  - Block RAMS are fundamentally 18Kb in size. Each block can also be used as two independent 9Kb blocks.
  - Each CMT contains two DCMs and one PLL.
  - Each DSP48A1 slice contains an 18x18 multiplier, an adder and an accumulator.