

## Virtex-6 LXT FPGAs

Optimized for High-performance Logic and DSP with Low-power Serial Connectivity  
(1.0 Volt, 0.9 Volt)

## Virtex-6 SXT FPGAs

Optimized for Ultra High-performance DSP with Low-power Serial Connectivity  
(1.0 Volt, 0.9 Volt)

	Part Number	XC6VLX75T	XC6VLX130T	XC6VLX195T	XC6VLX240T	XC6VLX365T	XC6VLX550T	XC6VLX760	XC6VSX315T	XC6VSX475T	
	EasyPath™ Cost Reduction Solutions <sup>(1)</sup>	—	—	—	—	—	—	—	—	—	
Logic Resources	Slices <sup>(2)</sup>	11,640	20,000	31,200	37,680	56,880	85,920	118,560	49,200	74,400	
	Logic Cells <sup>(3)</sup>	74,496	128,000	199,680	241,152	364,032	549,888	758,784	314,880	476,160	
	CLB Flip-Flops	93,120	160,000	249,600	301,440	455,040	687,360	948,480	393,600	595,200	
Memory Resources	Maximum Distributed RAM (Kbits)	1,045	1,740	3,040	3,650	4,130	6,200	8,280	5,090	7,640	
	Block RAM/FIFO w/ECC (36Kbits each)	156	264	344	416	416	632	720	704	1,064	
	Total Block RAM (Kbits)	5,616	9,504	12,384	14,976	14,976	22,752	25,920	25,344	38,304	
Clock Resources	Mixed Mode Clock Manager (MMCM)	6	10	10	12	12	18	18	12	18	
I/O Resources <sup>(5)</sup>	Maximum Single-Ended Pins <sup>(4)</sup>	360	600	600	720	720	1,200	1,200	720	840	
	Maximum Differential I/O Pairs	180	300	300	360	360	600	600	360	420	
Embedded <sup>(6)</sup> Hard IP Resources	DSP48E1 Slices	288	480	640	768	576	864	864	1,344	2,016	
	PCI Express® Interface Blocks	1	2	2	2	2	2	0	2	2	
	10/100/1000 Ethernet MAC Blocks	4	4	4	4	4	4	0	4	4	
	GTX Low-Power Transceivers	12	20	20	24	24	36	0	24	36	
Speed Grades	Commercial	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2, -3	-L1, -1, -2	
	Industrial	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1	-L1, -1	-L1, -1, -2	-L1, -1	
Configuration	Configuration Memory (Mbits)	26.1	43.5	61.4	73.6	95.8	143.7	184.4	104.2	156.3	
	Package <sup>(7)</sup>	Area									Available User I/O: SelectIO™ Interface Pins (GTX Transceivers)
	FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)										
	FF484	23 x 23mm	240 (8)	240 (8)							
	FF784	29 x 29mm	360 (12)	400 (12)	400 (12)	400 (12)					
	FF1156	35 x 35mm		600 (20)	600 (20)	600 (20)	600 (20)				
	FF1759	42.5 x 42.5mm			720 (24)	720 (24)	840 (36)		720 (24)	840 (36)	
	FF1760	42.5 x 42.5mm					1,200 (0)	1,200 (0)			

- Notes:
- EasyPath™ solutions provide a conversion-free, low-risk path for volume production. Please contact your Xilinx sales representative for information on Virtex-6 Family EasyPath device offerings.
  - A single Virtex-6 FPGA CLB comprises two slices, with each containing four 6-input LUTs and eight Flip-Flops (twice the number found in a Virtex-4 FPGA slice), for a total of eight 6-LUTs and 16 Flip-Flops per CLB.
  - Virtex-6 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
  - Digitally Controlled Impedance (DCI) is available on I/Os of all devices.
  - I/O standards supported: HT, LVCMOS (2.5V, 1.8V, 1.5V, 1.2V), LVTTTL, HSTL I (1.2V, 1.5V, 1.8V), HSTL II (1.5V, 1.8V), HSTL III (1.5V, 1.8V), LVDS, Extended LVDS, RSDS, Bus LVDS, LVPECL, SSTL I (1.8V, 2.5V), SSTL II (1.8V, 2.5V), SSTL (1.5V).
  - One system monitor block included in all devices.
  - All products available Pb-free and RoHS-Compliant (FFG).